UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/679,594	10/06/2003	Neil Johnson	ALT.P026	5941

27296 7590 09/27/2007

LAWRENCE M. CHO
P.O. BOX 2144
CHAMPAIGN, IL 61825

EXAMINER	
FARROKH, HASHEM	
ART UNIT	**PAPER NUMBER**
2187	
MAIL DATE	**DELIVERY MODE**
09/27/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Advisory Action Before the Filing of an Appeal Brief	Application No. 10/679,594	Applicant(s) JOHNSON, NEIL	
	Examiner Hashem Farrokh	Art Unit 2187	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 04 September 2007 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☒ The period for reply expires 6 months from the mailing date of the final rejection.
   b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☒ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: *38-51*.
   Claim(s) objected to: _____.
   Claim(s) rejected: *16,18,20-24,26,27,33-35 and 37*.
   Claim(s) withdrawn from consideration: *1-15,17,19,25,28-32 and 36*.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☐ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: _____.
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08) Paper No(s). _____
13. ☒ Other: See Continuation Sheet.

HR
9/21/07

Brian R. Peugh
Primary Examiner
9/25/07

Continuation of 13. Other:
Claims 16, 18, 20-21, 23-24, 26-27,33-35, and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5, 867,727 to Hattori in view of U.S. Patent No. 5,557,750 to Moore et al. (hereinafter Moore) and U.S. Patent No. 6,615,296 B2 to Daniel et al. (hereinafter Daniel).
Claim 16 recites:
"(a) A method for managing data, comprising: selecting a first first-in-first-out (FIFO) memory from a plurality of (FIFO) memories to output first data stored in a first storage element in the first FIFO memory in response to a first read address from a data reading device,
(b) wherein the first data was prepared for output prior to a generation of the first read address from the data reading device;
(c) preparing next data from a next storage element from the first FIFO memory for output by transmitting a read address of the next storage element to the first FIFO memory prior to a request for the next data from the data reading device." (Tags a, b, and c are added).

As shown above the claim comprises 3 portions or limitations which are tagged as a, b, c. Hattori teaches limitation (a) but not limitations (b) and (c). Moore teaches limitation (b) but not limitations (a) and (c). Daniel teaches limitation (c) but not limitations (a) and (b). But the combination of Hattori, Moore, and Daniel teach all the limitations (a), (b), and (c).

In page 11 of the Remarks, the Applicant states:
"The Office Action mailed 6/4/2007 acknowledges that Hattori does not teach selecting a first FIFO memory From a plurality of FIFO memories to output first data stored in a first storage element in the first FIFO memory in response to a first read address from a data reading device, wherein the first data was prepared for output prior to a generation of the first read address from data reading device"
The above statement is only partially correct since Hattori teaches:
"The Office Action mailed 6/4/2007 acknowledges that Hattori does not teach selecting a first FIFO memory from a plurality of FIFO memories to output first data stored in a first storage element in the first FIFO memory in response to a first read address from a data reading device,"
In page 11 to page 12 of the Remarks, the Applicant further states:
"Moore discloses a pre-fetch register 135 which lies between a host and a main FIFO 132. Data in this register 135 is fetched from the main FIFO 132 during available internal data bus cycles. This allows the data to be available when the host requests it. Applicant submits that the pre-fetch register 135 is operable to pre-fetch data from only a single FIFO such as main FIFO 132, not a plurality of FIFO memories as required by the claimed invention (Moore col. 1, line 67 through col. 2, line 7, col. 3, lines
54-62). Thus, Moore teaches away from selecting a first FIFO memory from a plurality of FIFO memories to output first data stored in a first storage element in the first FIFO memory in response to a first read address from a data reading device, wherein the fir~ data was prepared for out3ut prior to a generation of the first read address from the data reading device. Applicants submit that a prior art reference must be considered in its entirety, i.e. as a whole, including portions that would lead away from the claimed invention."

The limitation or feature that the Applicant argues about is limitation (b) above, which states:
"wherein the first data was prepared for output prior to a generation of the first read address from the data reading device;"
This limitation taught by Moore and as recited does not requires a plurality of FIFO memories. The Disclosure by Moore is not used to teach a plurality of FIFO memories. The first reference or Hattori teaches a plurality of FIFO memories. Moore is used to teach prefetching the data from a FIFO, prefetching does not require plurality FIFO memories as seems the Applicant to imply. The Examiner disagrees with the allegation that Moore teaches away from Hattori.
In page 12 of the Remarks, the Applicant states:
"Daniel discloses providing an RD pointer that points to a next location within a FIFO to be read from. The RD pointer is maintained by an off-board processor which communicates with the FIFO across the bus (Daniel Abstract, co]. 4, lines 40-49, and col. 6, lines 34-37). The RD pointer is a requester for next data from a data reading device. Daniel does not disclose preparing next data for output prior to a request
for the next data from the data reading device.
Furthermore, the techniques described in Daniel are also operable only with a single FIFO, not a plurality of FIFO memories as required by the claimed invention (Daniel Figures 3A-3F and 4A-4F). Thus, Daniel also teaches away from electing a first FIFO memory from a plurality of FIFO memories to output first data stored in a first storage element in the first FIFO memory in response to a first read address from a data reading device, wherein the first data was prepared for output prior to a generation of the first read address from the data reading device."

As Daniel was used to teach the limitation (c) which recites:
"preparing next data from a next storage element from the first FIFO memory for output by transmitting a read address of the next storage element to the first FIFO memory prior to a request for the next data from the data reading device."

This limitation does not require that the limitations (a) and (b) to be presence, if Daniel, in addition to limitation (c), taught limitations (a) and (b), then claims would have been rejected under 102. Under 103 rejections, it is not necessary that all references teach or include all limitations as appears to be suggested by the Applicant. Since the limitations (b) and (c) can be used for a single FIFO or plurality of FIFOs, the Examiner disagree with the Applicant that Moore and/or Daniel teaches away from Hattori or one another. The independent claims 23 and 33 have similar limitations and the Applicant uses a similar argument to object the reject of these claims. Therefore, the same response gives above for claim 16 applies to claims 23 and 33.

In summary, the Examiner believes the combination of Hattori, Moore , and Daniel teach all limitations recited in the claims and therefore the Examiner maintains his position. .